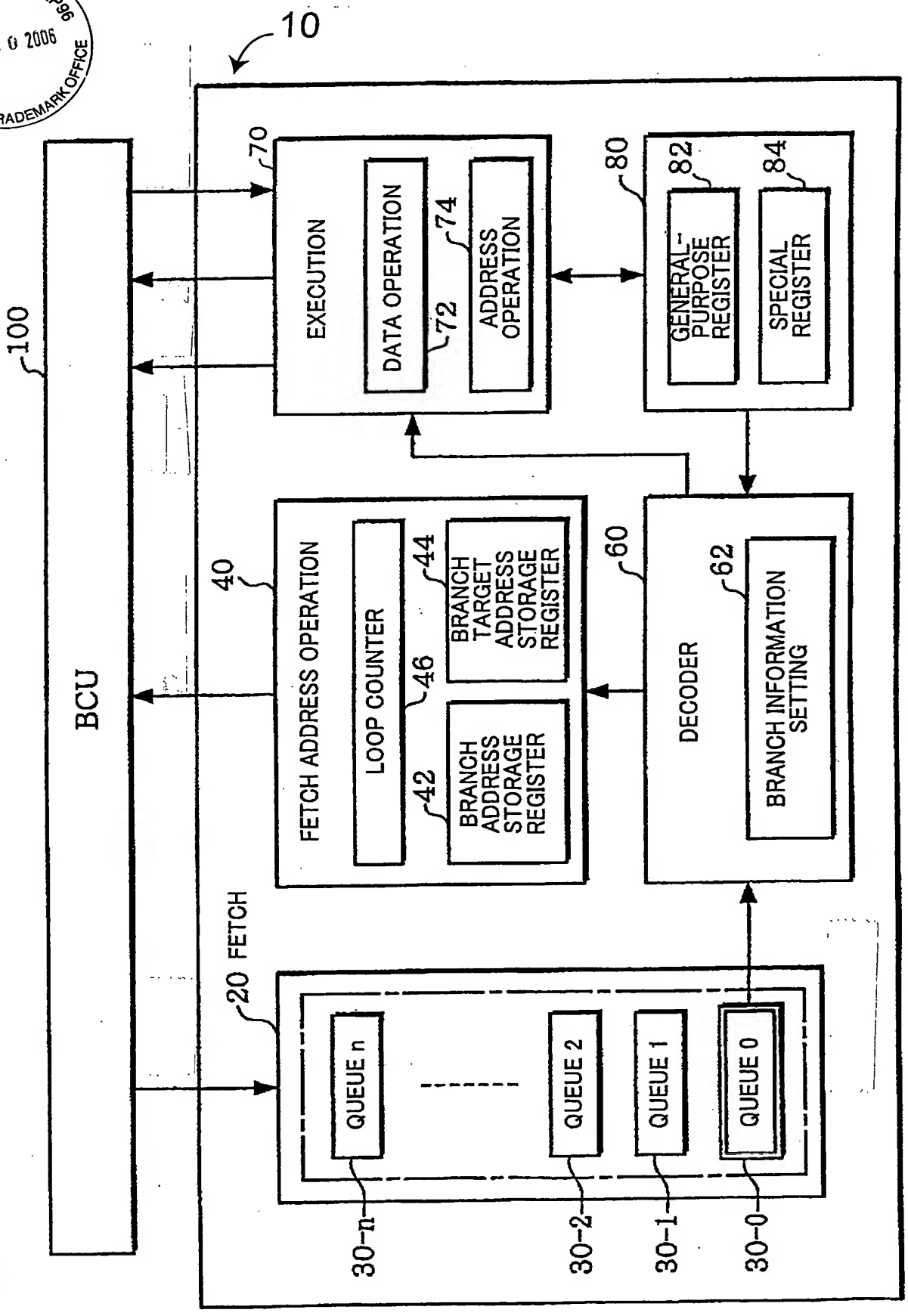


FIG. 2

FIG. 3A

```
jppr  x, y
```

FIG. 3B

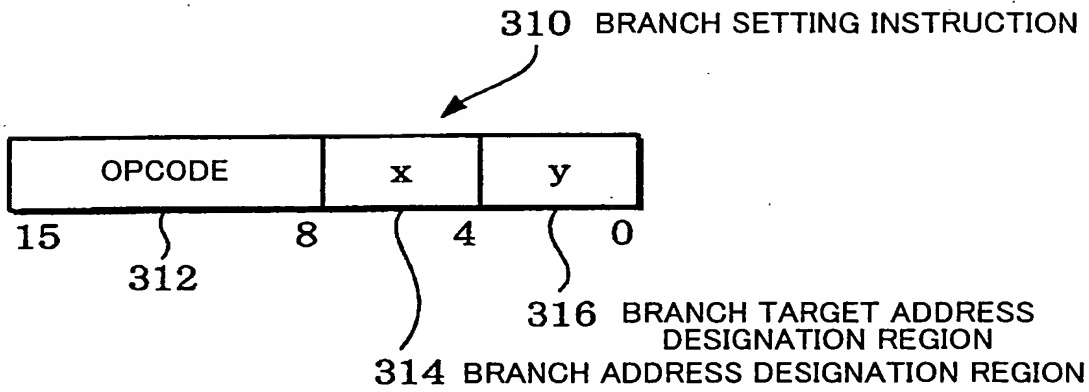


FIG. 3C

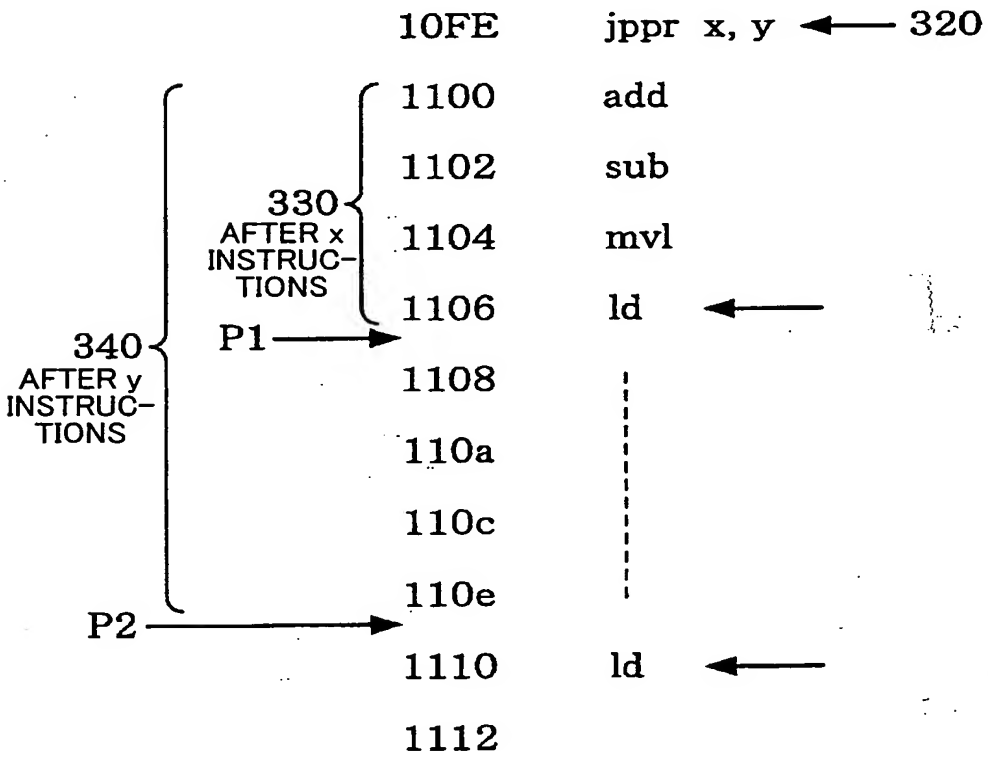


FIG. 4

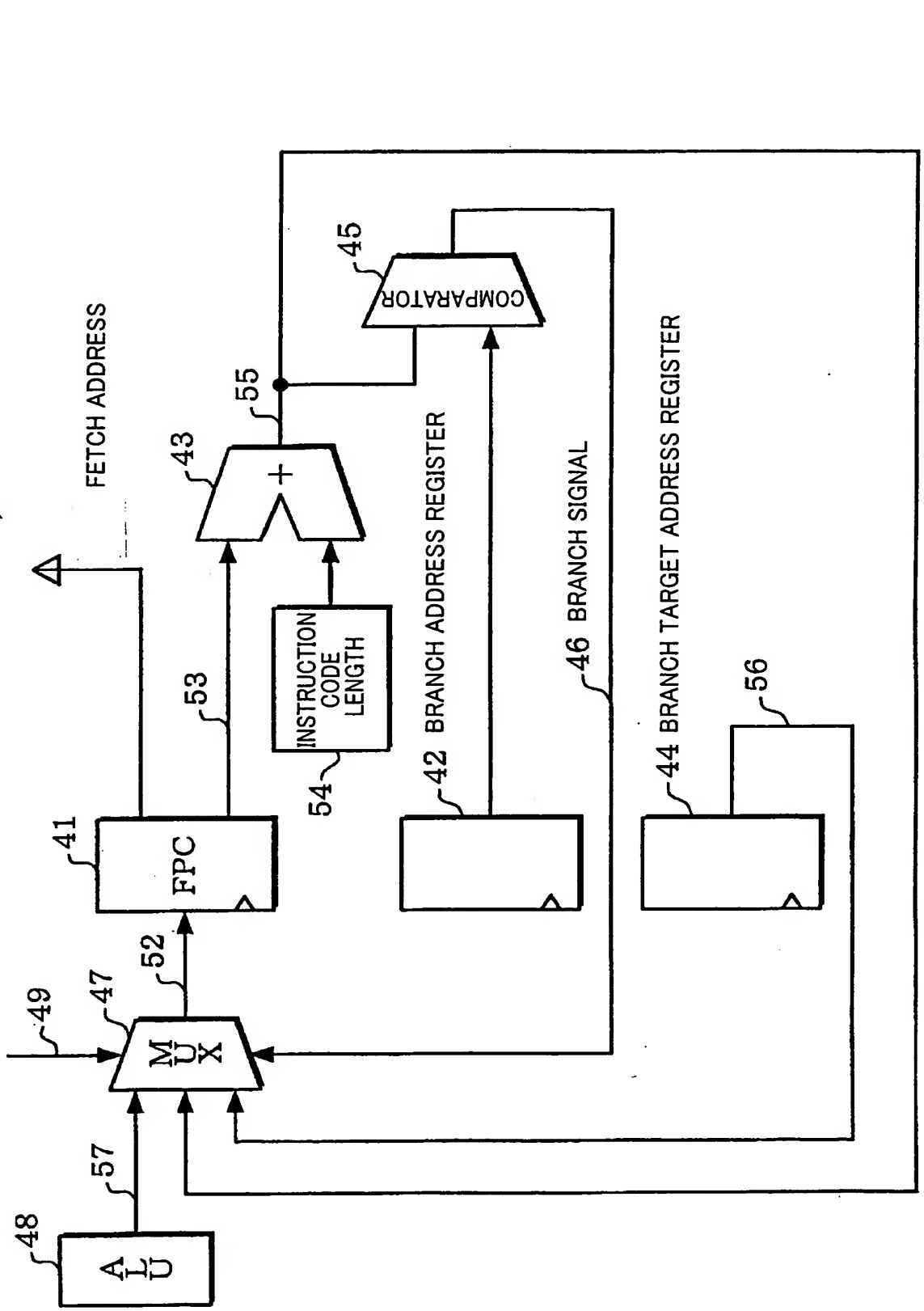

40 FETCH ADDRESS OPERATION CIRCUIT
FETCH ADDRESS
45
COMPARATOR
55
43
+
INSTRUCTION CODE LENGTH
54
53
42 BRANCH ADDRESS REGISTER
46 BRANCH SIGNAL
44 BRANCH TARGET ADDRESS REGISTER
56
41
FPC
52
47
49
MUX
57
48
ALU

FIG. 5A

```
loop  x, y, z
```

FIG. 5B

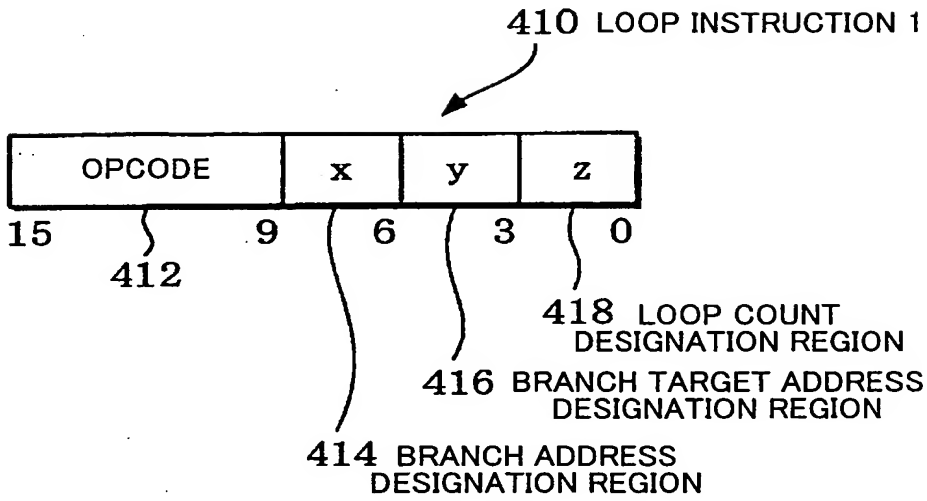
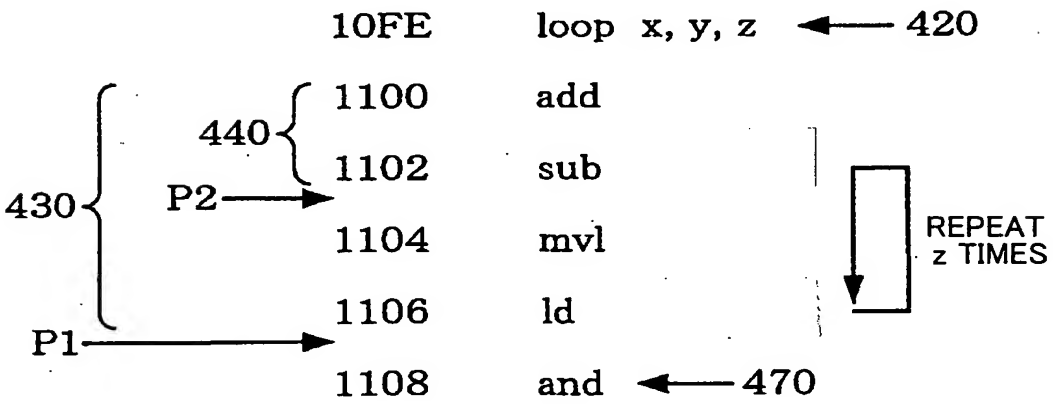


FIG. 5C



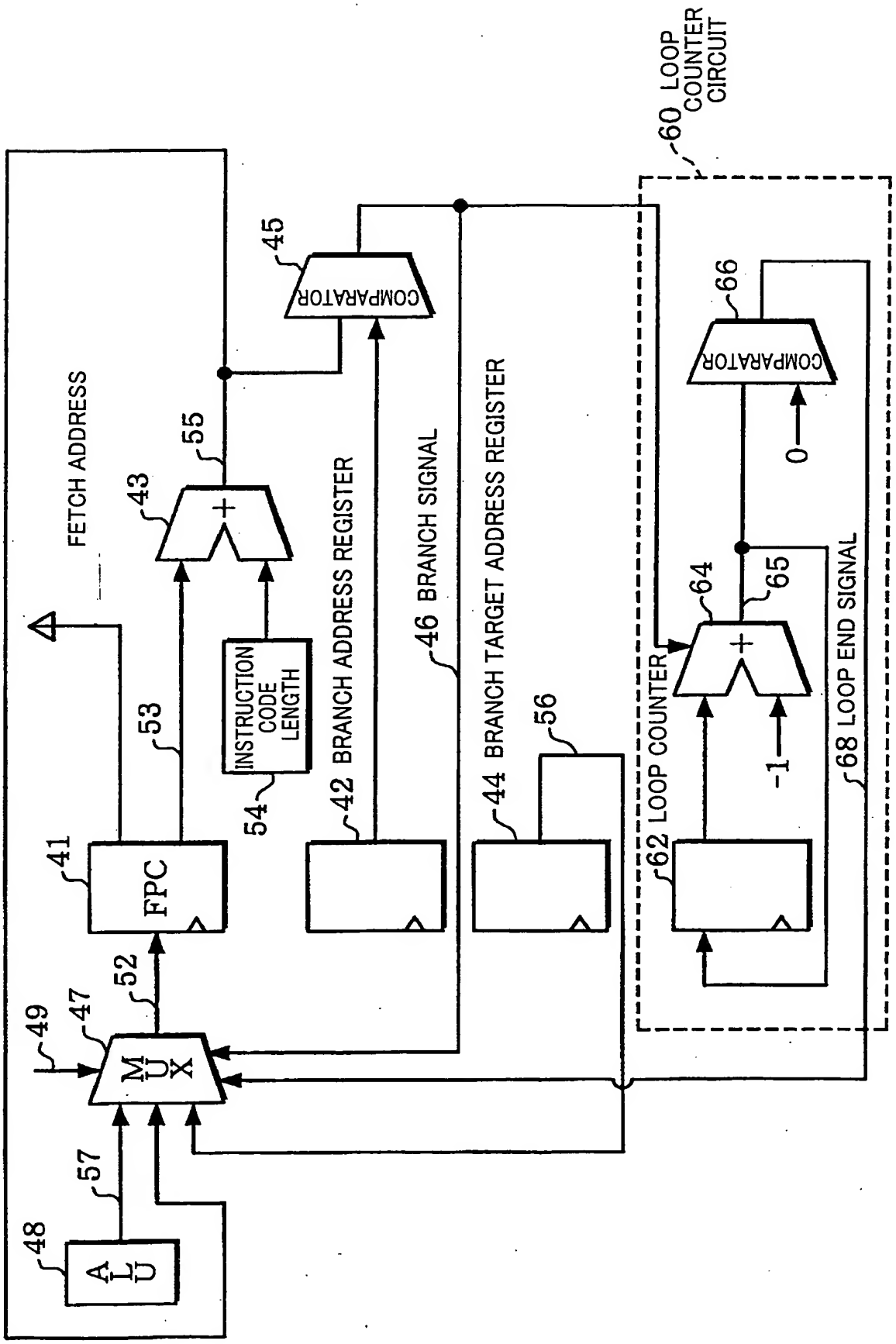

40' FETCH ADDRESS OPERATION CIRCUIT
60 LOOP COUNTER CIRCUIT
FETCH ADDRESS
45
COMPARATOR
66
COMPARATOR
0
55
43
+
INSTRUCTION CODE LENGTH
54
42 BRANCH ADDRESS REGISTER
46 BRANCH SIGNAL
44 BRANCH TARGET ADDRESS REGISTER
56
64
65
+
62 LOOP COUNTER
-1
68 LOOP END SIGNAL
53
41
FPC
52
49
47
MUX
57
48
ALU

FIG. 6

FIG. 7A

```
loop  x, z
```

FIG. 7B

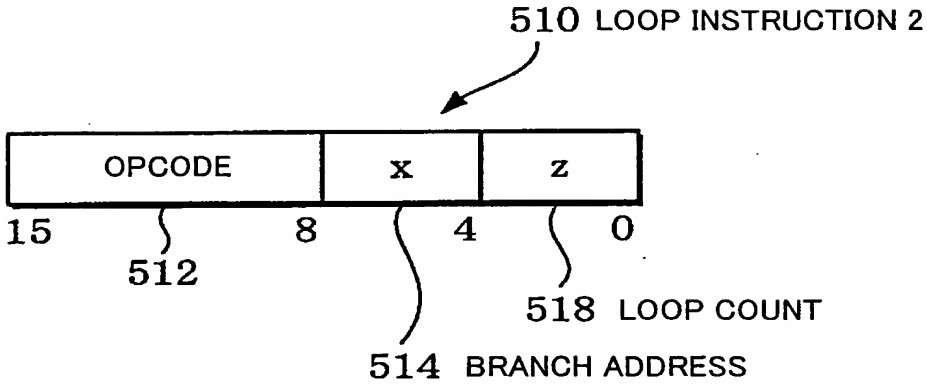


FIG. 7C

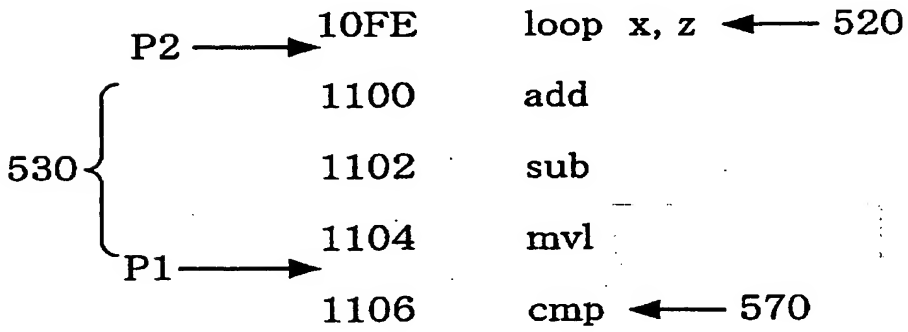


FIG. 9A

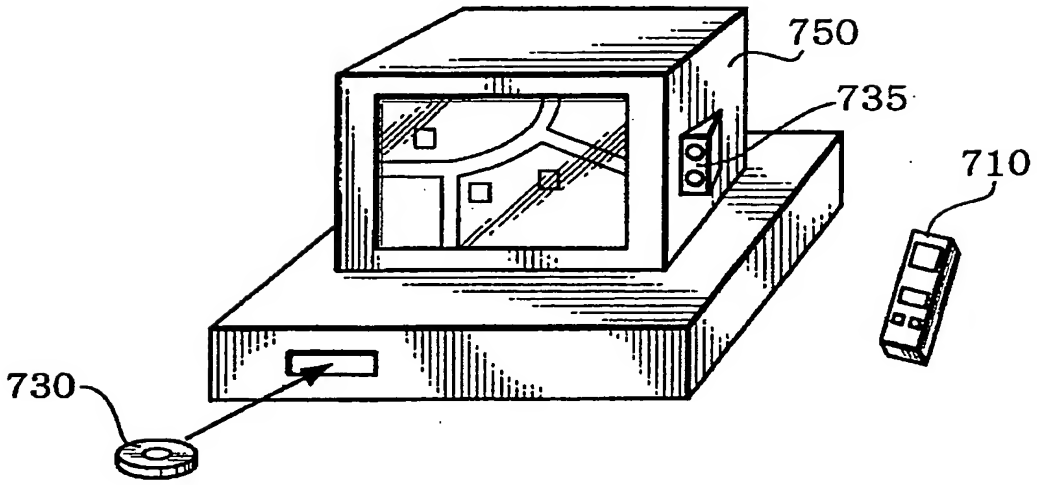


FIG. 9B

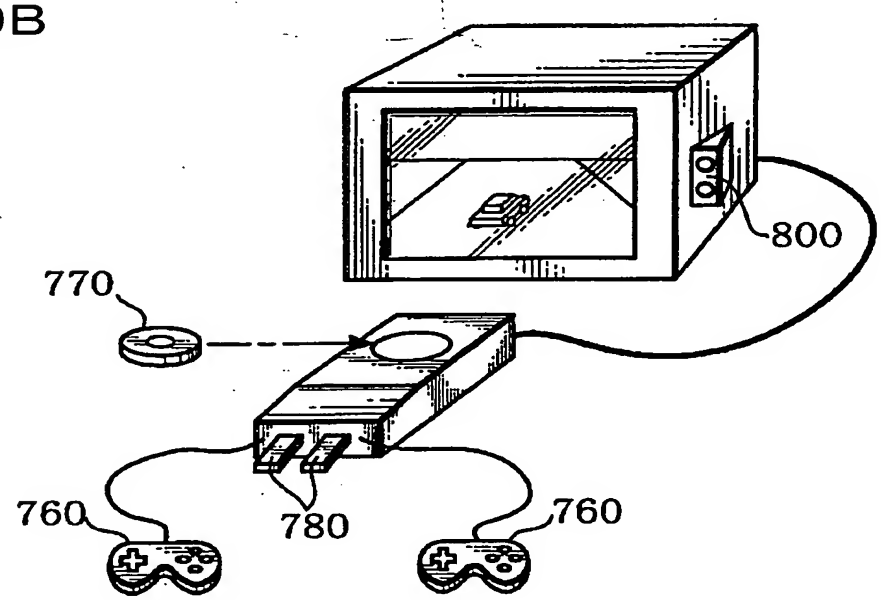


FIG. 9C